Recent FE-B Module Experience at LBL

K. Einsweiler, LBNL

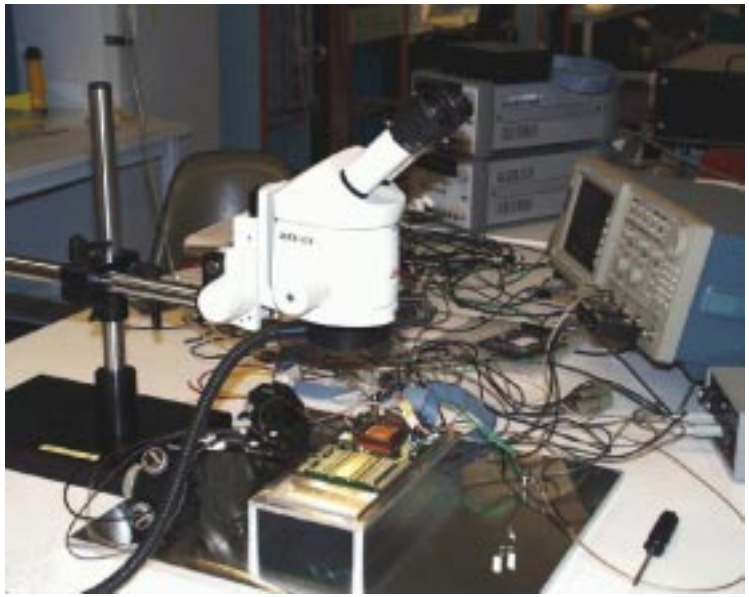
Status and results from first two FE-B modules

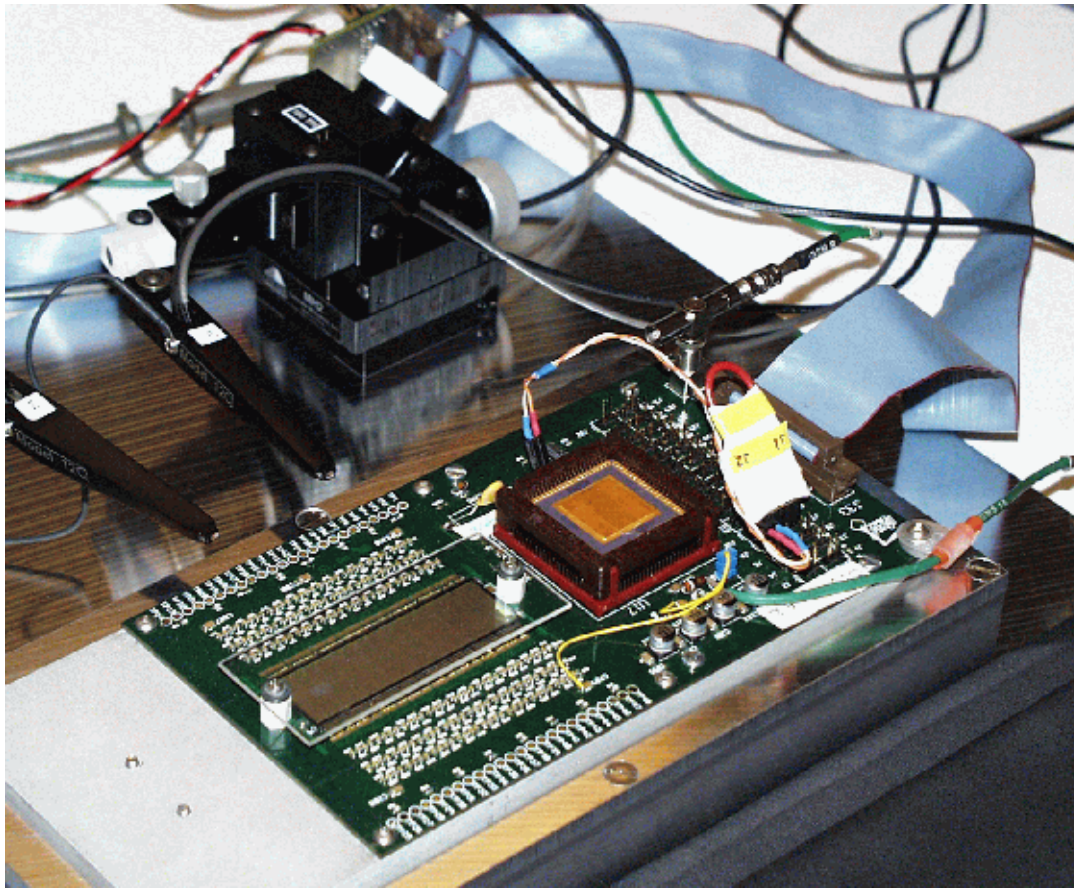
First impressions from Flex hybrid module tests

Status of FE-B “non-hybrid” modules

- Two modules were flipped by Boeing in June, and assembled using the Genova Module Support Card (12 layer PC card which makes all of the necessary

interconnections between 16 FE chips and MCC).





Some features of the Module Support Card:

- Decoupling using 0.01 μF is present for all 9 bias points (8 DACs and MON_REF) on each FE chip.
- Decoupling using 0.01 μF is present for each of the 3 LV supplies on each FE chip
- Hitbus from each chip is brought to a patch point for jumper-selection of this signal to PLL for self-triggered readout, but it is not buffered to transmit off of the board
- Only internal charge injection is supported (static VCal plus strobe). Modifications needed for external injection (external chopping of VCal).
- Three planes exist in the board: DGnd, AGnd, and AVdd. AVcc and DVdd are distributed by U-shaped bus.
- Detector connections (DGUARD and DGRID) are AC coupled to AGnd. A jumper-selected DC connection is needed.

Summary of the two FE-B modules:

- After some wire-bonding problems were fixed, both modules work perfectly from the digital point of view: all 16 chips have every channel working when using digital hit injection.
- When the detector is biased, and the FE-B DACs are set to standard conditions, the power consumption is very stable and reproducible (for 16 FE-B plus MCC):

  DVdd uses 400 mA at 3.5V (about 20 mA per FE-B plus 80 mA for MCC) = 1.4W

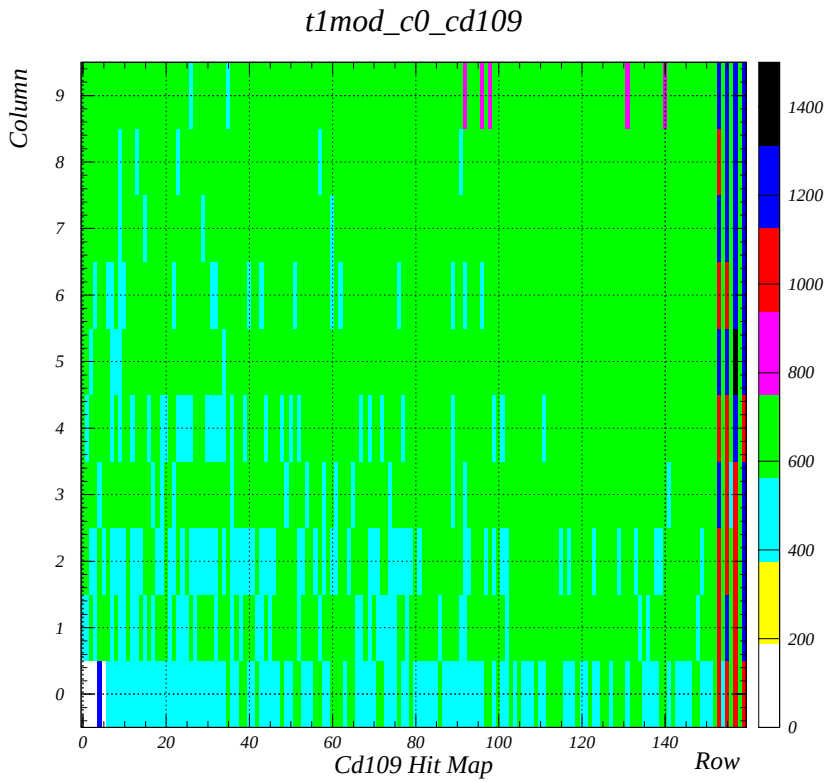
  AVdd uses 650 mA at 3.5V (about 25 mA per FE-B in front-end, rest in Hitbus buffers) = 2.3W

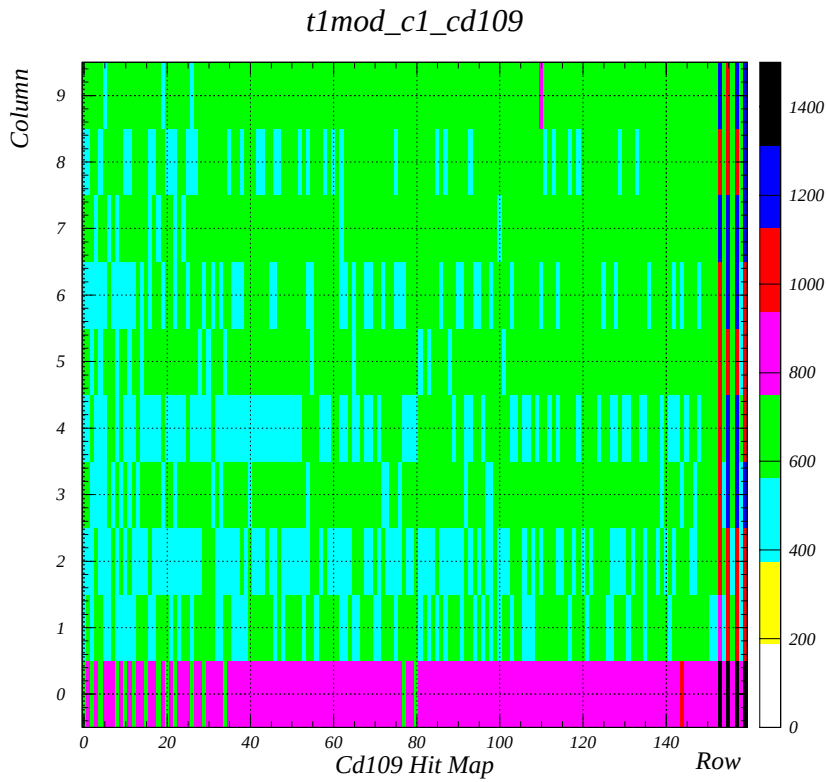
  AVcc uses 250 mA at 1.75V = 0.4W

  A total of about 4.1W, with 40μW/pixel in analog FE
- One module uses a CIS Tile2 detector, and the other is a Seiko Tile1 detector. Both are 1M. The detector currents are quite high at -150V. The Tile1 uses about 45μA and the Tile2 about 200μA.
- The Tile1 module has only a few dead channels, with the exception of one chip (Chip 14) which has about 140 dead channels, mainly in the first two columns. Here, dead means that when doing a threshold scan, these channels produce essentially no hits.
- The Tile2 module has many dead channels, mainly in the chips on one side (a total of about 800 bad channels are found, most of them in Chips 0 and 4).

Tile1 Module Results:

- Source maps were made for each chip before doing TDAC tuning of thresholds (threshold about 4.5 Ke):



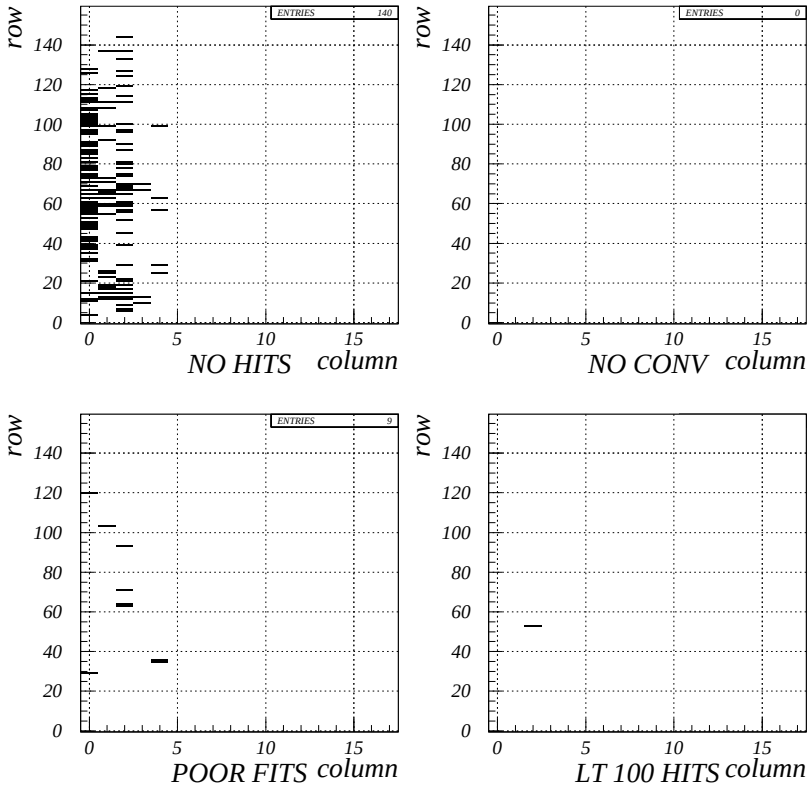


- Note Chip 0 and 8 in Tile have Column 0 400μ long, all others have 600μ.

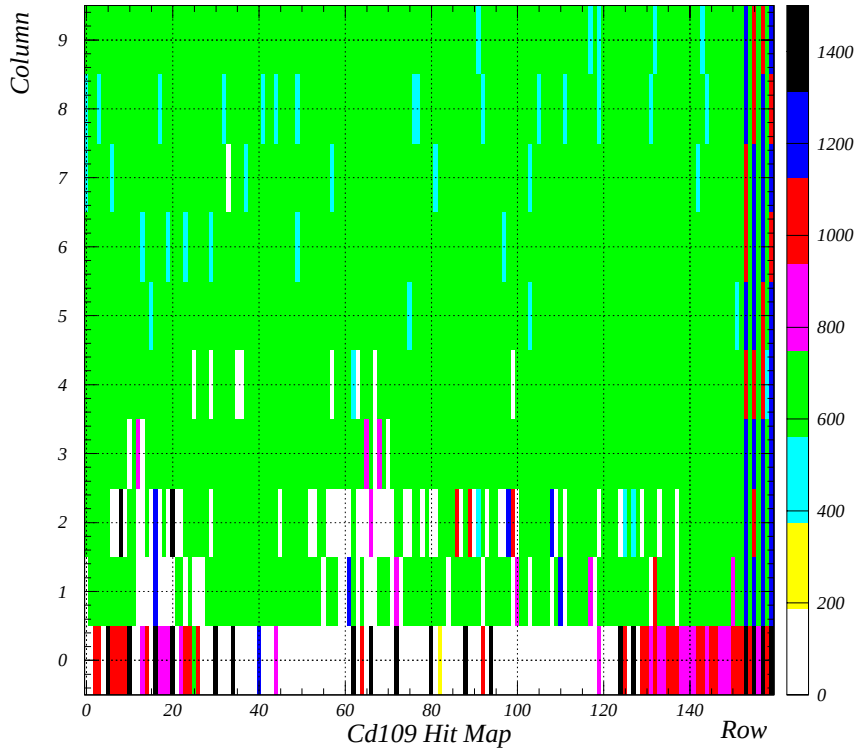
Bad Chip 14 in Tile 1:

- Both charge injection and source run show similar behavior:

t1mod_c14_tune

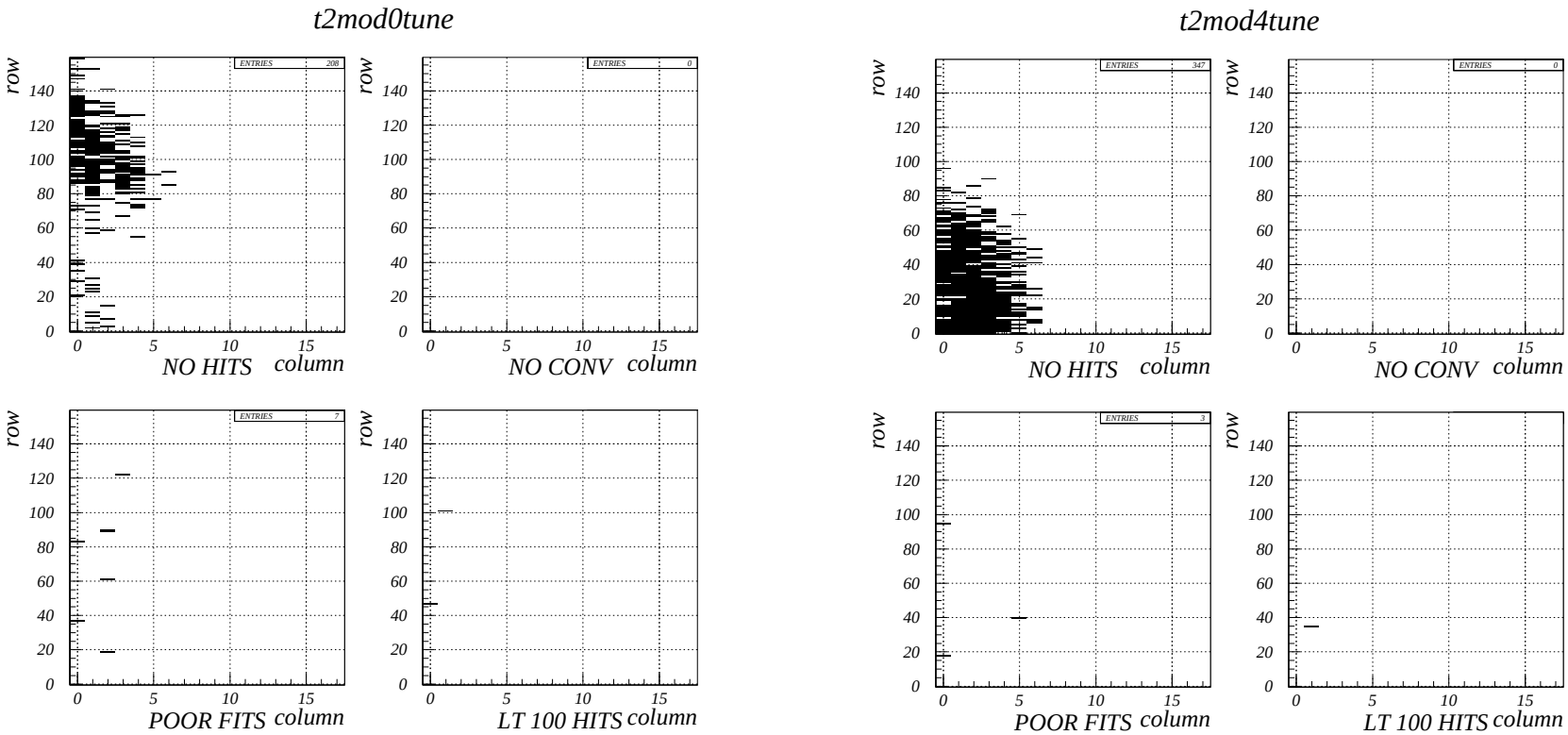


t1mod_c14_cd109



Tile 2 module results:

Examples of two bad chips from charge injection:



General Observations on Modules

Two major differences relative to single chip operation:

- Significant noise increase for comparable operating point
- Instability of operation observed

Instability:

- For basic module support card, fully bonded, find that module can enter a “high current” state in which I(AVdd) increases from about 650 mA to about 900 mA.
- This seems to correspond to most or all channels in the full module “oscillating”. This is easily seen on the Hitbus, or when doing a threshold scan and finding many hits below threshold.
- When the module is initially powered without HV bias, and then subsequently bias is applied, the module may enter this state.
- When injecting charge in many pixels, the module may enter this state. In particular, in earlier versions of PixelDAQ, when scanning many chips on one run, the strobe and readout masks for earlier chips in the run were left on. This would result in a pattern where after scanning several chips, the module would enter the high current state.
- Bringing the module out of this state required setting FE bias DACs down to shut off front-ends (CINDAC and D1DAC in FE-B).

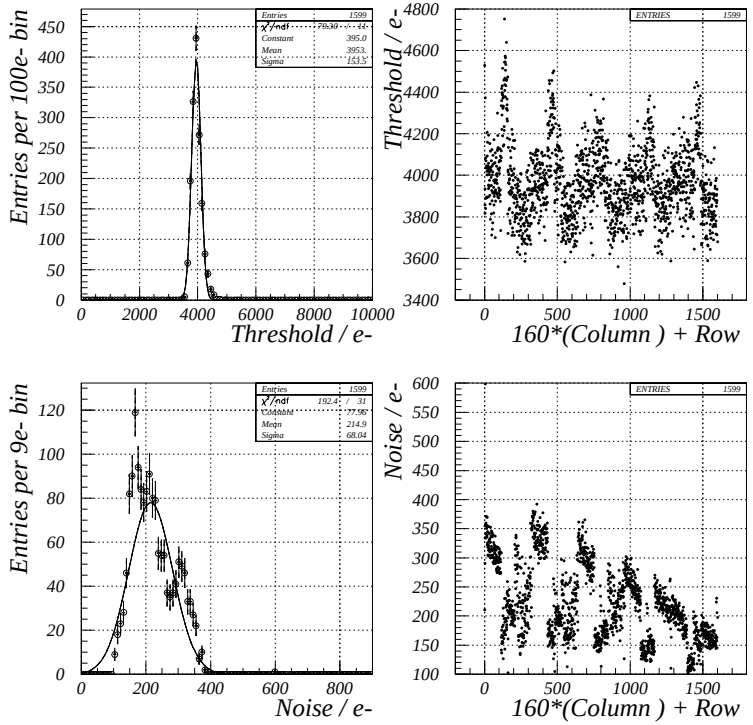
High Noise:

- For most studies, the preamplifier feedback current (FPDAC or DAC1 in FE-B) was set to 5, corresponding to about 1.5 μs return to baseline for 20Ke charge. At this operating point, we typically observe about 110e of noise on both ST1 and ST2 detectors (single chip devices on the single chip support card).
- For the modules, noise values in the range of 150e up to even 400e or 500e have been observed. These measured noise values change significantly from one threshold scan to the next in an apparently random way. Sometimes, there is even a corresponding “column-dependent” threshold shift observed.

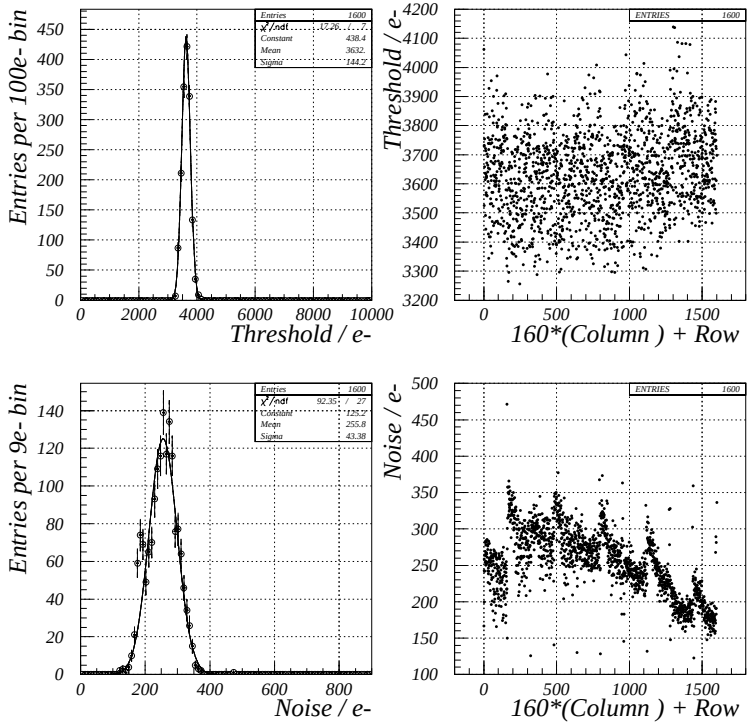
Examples from Tile 1 Module

Two examples of chips which were noisy:

t1mod_c0_tune

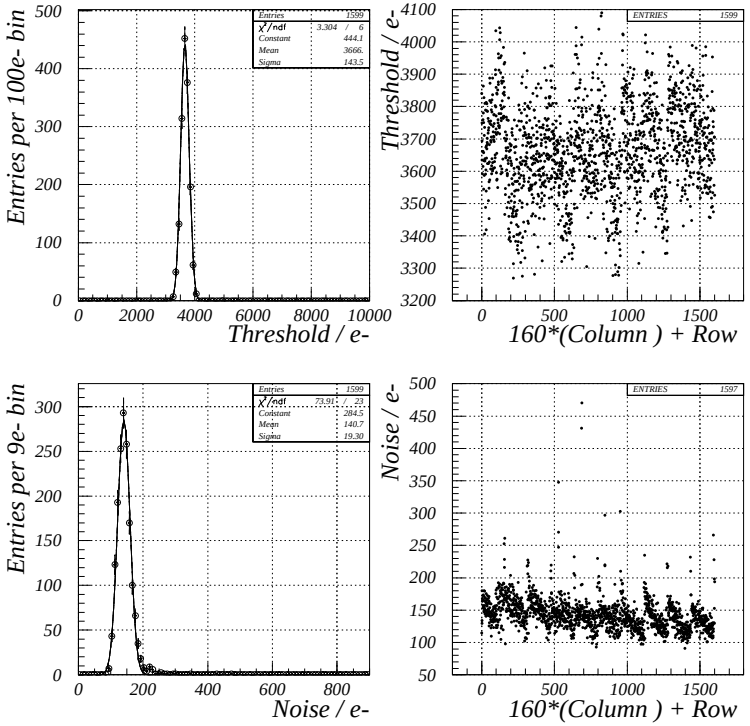


t1mod_c4_tune

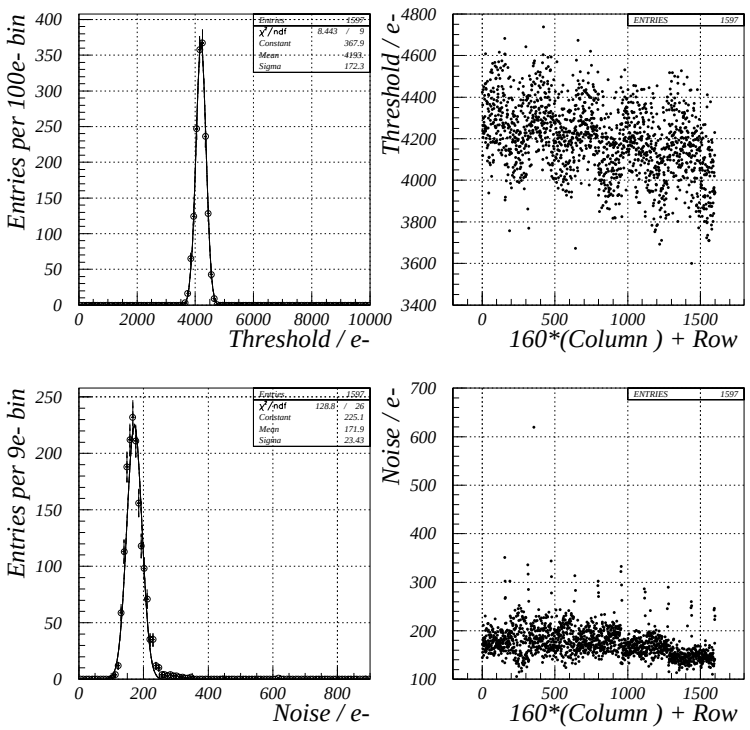


Two examples of chips which were not so noisy:

t1mod_c10_tune

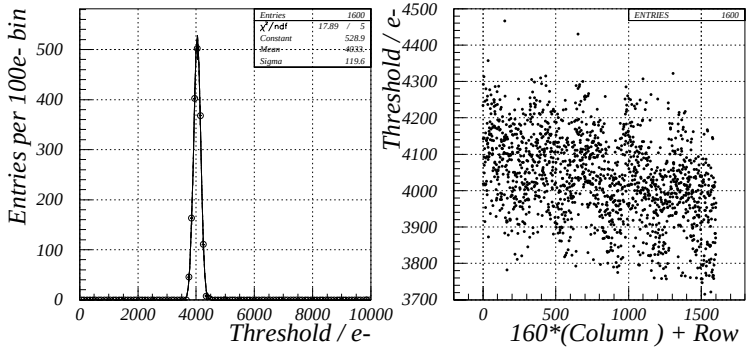


t1mod_c15_tune

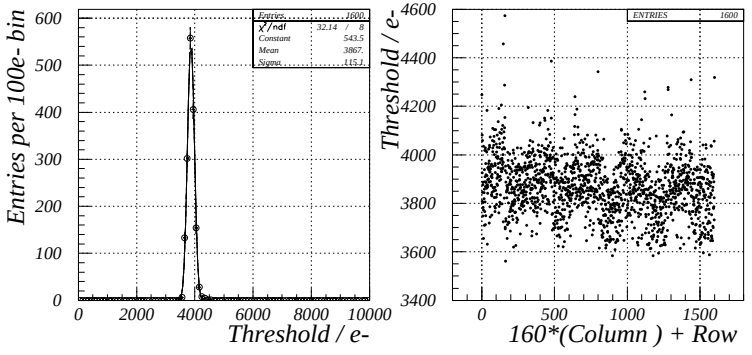


Examples from the same chip a few minutes apart:

t1mod_c3_tune1



t1mod_c3_tune3



Module Concerns

Many ways for there to be “coherent” effects that do not show up in single chip assemblies:

- FE chips can communicate via power supply lines if the decoupling is not adequate. In the present module support card, they can also communicate via the bias decoupling points as well.
- FE chips can communicate via large sensor substrate, especially through shared structures (p-stops, guard rings, etc).
- The noise levels on the LV or HV supplies can be larger due to PC board layout or other reasons.
- There can be more analog-digital cross-talk within the chips because of poor substrate contacts.
- There can be greater coherent digital activity (all 16 chips have a clock with the same phase) induced on the shield in FE-B which could couple into the detector or into AGnd.

Some tests on a single chip card:

- Took a high quality ST2 detector and scanned repeatedly, checking stability of threshold and noise behavior.
- Removed wire bonds to external decoupling on 9 bias nodes. No difference was observed.
- Removed LV decoupling capacitors close to the FE chip (there are two sets of 3 caps close to the chip).
- These modifications made no difference at all in the threshold and noise behavior, and the chip was always stable and quiet.
- The wire-bond connecting the Shield to AGnd was removed (Shield is M3 layer above the digital readout circuitry in the active area of the array). This was disastrous. The chip practically oscillated whenever even a single pixel was injected with a 3Ke threshold. Making the Shield connection to DGnd instead of AGnd made no difference in the noise or threshold behavior.

Conclude:

- On single chip, there is no need for the bias decoupling, and the connection of Shield to a low impedance ground is very important.

Some tests on Tile1 module card:

- Normally operate the module with charge injection into a single chip only. The other 15 chips have injection and readout disabled for all pixels.
- Normally set thresholds on all non-injected chips to TDAC=7 (maximum local threshold for FE-B).
- Tried “shutting down” the front-end in the non-injected chips by setting CINDAC and D1DAC to 1 (negligible bias in the input transistor and the diffamp). Under these conditions, it is impossible to generate a normal hit from the front-end via charge injection.
- Tried wire-bonding RST to DGnd on 15 of the chips on the module. On FE-B this has the effect of shutting down the timestamp generation, and holding all pixels in a reset state so there can be no digital activity in the active array.
- Tried removing the XCK connection on 15 chips. This even kills all digital activity in the periphery of the chip.
- None of these modifications had a significant effect on the high noise behavior observed in the chip under test. Its noise would still vary between 150e and 400e from one threshold scan to the next.

Not able to improve the module performance to that of the single chip performance...

Modifications made to the Tile1 module card:

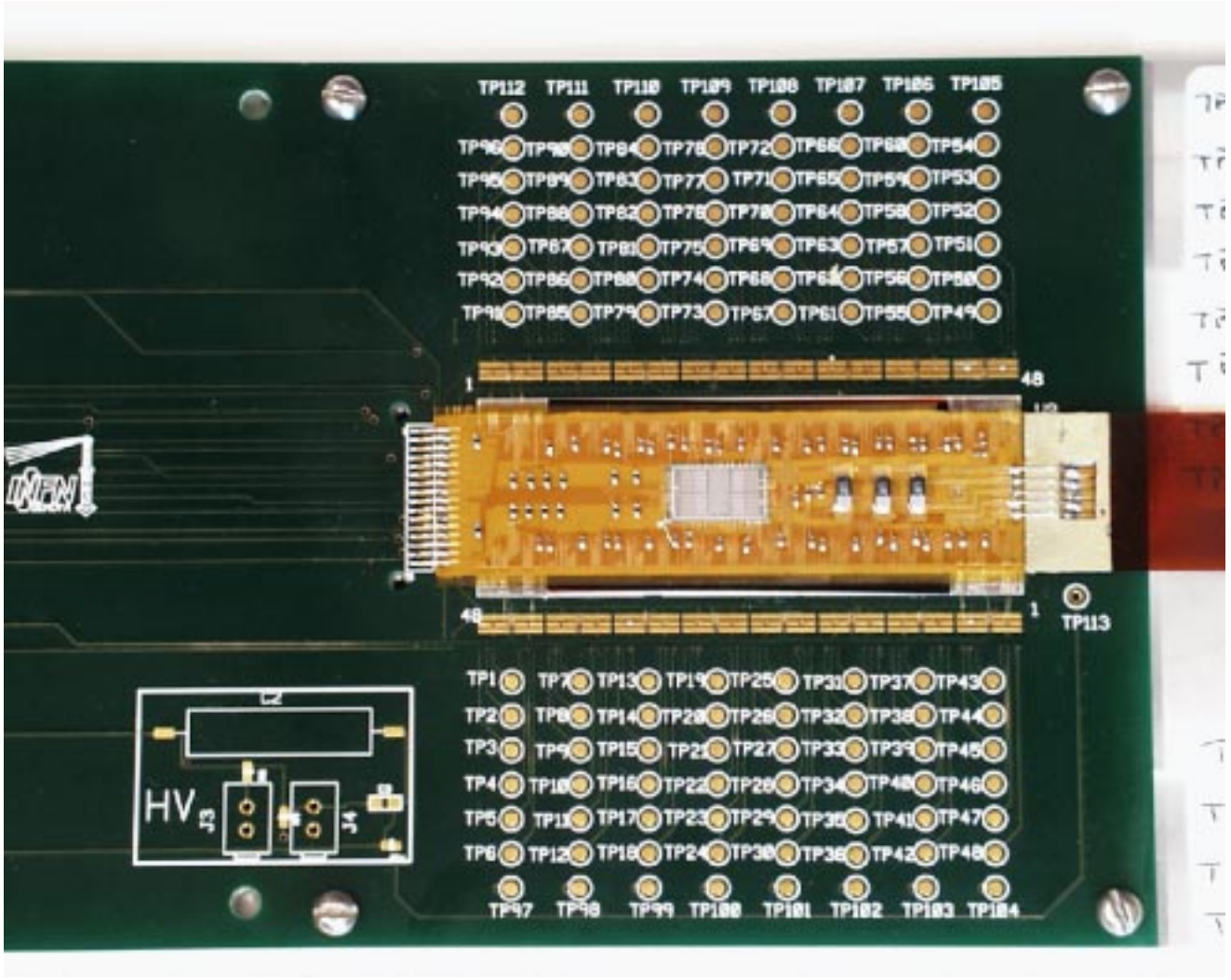
- Added piggy-back 0.1 μF capacitors by each chip in parallel with existing 0.01 μF capacitors.
- Removed wire-bonds from 9 bias nodes on each chip (8 current DACs plus MON_REF). On one module this was done on one side only. On the Tile1 module it was done on both sides (all chips).
- Improved AGnd to DGnd connection near chips by soldering a wire across the ground side of the LV decoupling capacitors.
- This essentially eliminated the instability problem. It was possible to operate the module consistently with all chips tuned (TDACs set for minimal dispersion) and a threshold of about 3.5Ke, while injecting all chips simultaneously. This was previously impossible.

Suggests that the decoupling on the existing support cards is not adequate...

- A 0.1 μF MLC capacitor typically has an ESR of less than 1Ω in the frequency range of a few hundred KHz to a few MHz of most interest to us. A 0.01 μF capacitor is most effective above 10 MHz where we are not sensitive. It is possible to get such capacitors in 0402 packages, but for a good dielectric, an 0603 package is needed...

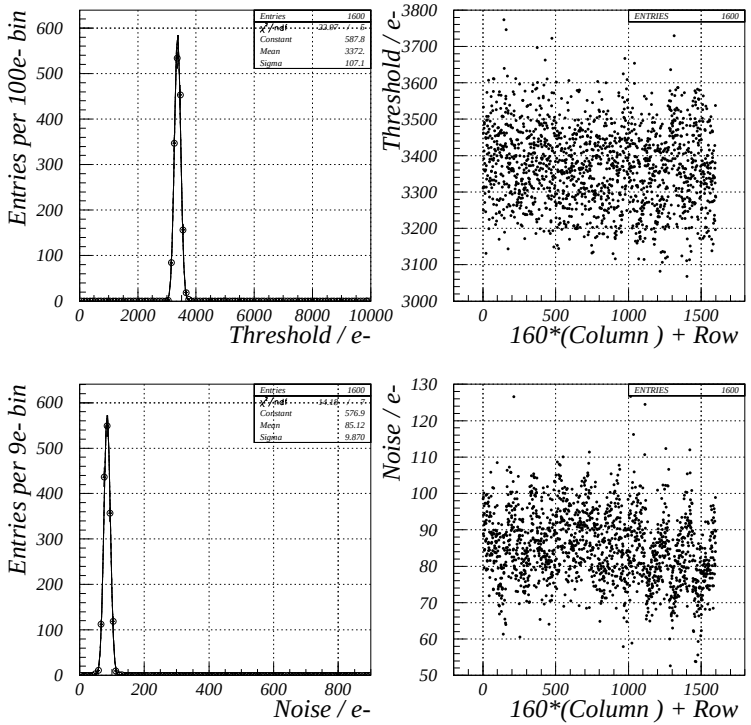
First Experience with UOK Flex

- First test done was to build a simple module with 4 bare FE-B die, and connect a Flex with MCC and components to this:

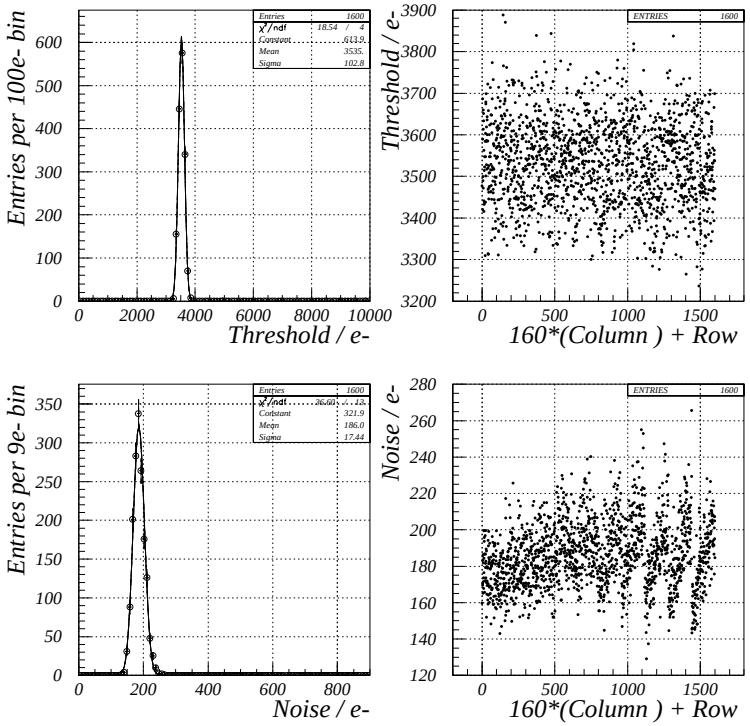


- This flex and MCC worked OK, but some of the chips were noisier than expected. An example of one chip scanned twice:

flex0tune1

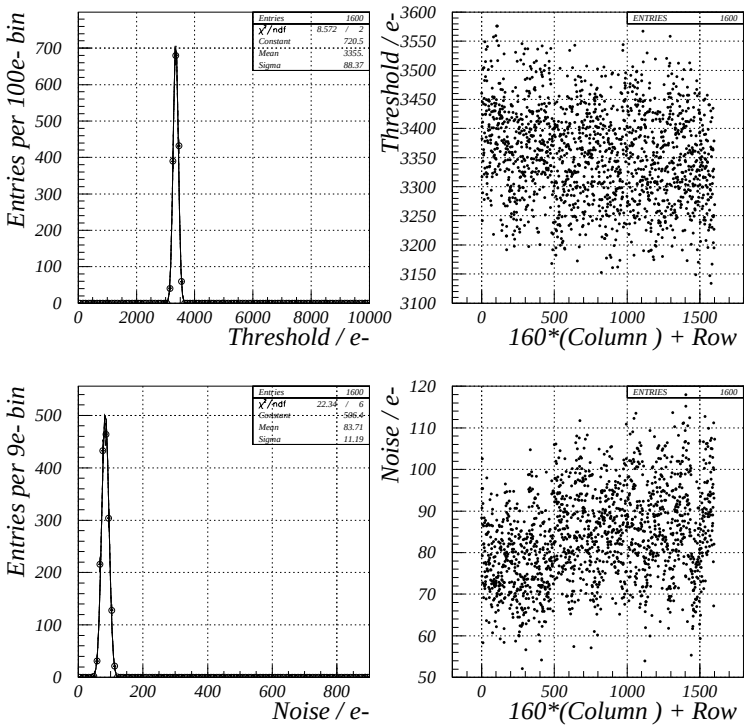


flex0tune3

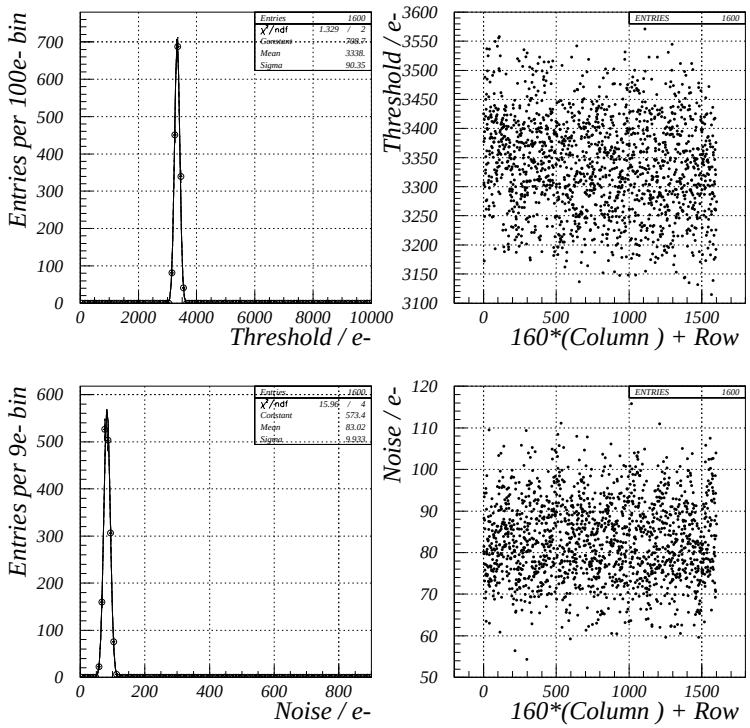


- An example of a different chip which shows stable low noise behavior:

flex15tune1



flex15tune3



- <u>One lesson from this:</u> in the single chip cards, the chips were always attached with conducting epoxy, whereas in the modules, we used Dow340 plus UV-cure epoxy (insulating). For the Flex, we used conducting epoxy, and it still shows qualitatively similar noise effects to the full module. Probably the substrate contact method is not the problem...

First results on a complete Flex module:

- Module was the last Boeing module, which was build using a CIS Tile1 detector and chips from a wafer that had been thinned to 150µ by GDSI. The thinning was done by cutting the wafer in half after bumping, protecting the bumps, and back-grinding. The dicing was done by GDSI. We had fun pulling the die off the dicing tape (tweezers don't work on such thin die...) The flip-chipping was done without any problems by Boeing.
- The Flex module assembly was completed on Weds this week and hand-carried here by Gil.
- It was tested for the first time last night, and all 16 chips work perfectly as far as register tests and digital injection is concerned. The digital injection tests were performed in full MCC mode, so the MCC also works. The detector bias is connected (tested by forward-biassing), and the current at 135V is negligible. The VCal line is not connected on the Flex and must be bonded separately down to the support card. This has not yet been done, so it is not possible to test the analog performance (noise, threshold) of the module yet...
- Stay tuned for more details...

Comments on first Flex experience:

Congratulations to Rusty, UOK, Genova on job well done !

Modifications needed for "user friendliness":

- Longer bonding pads, placed further from the MCC
- Put DGnd pad under MCC for backside contact, and move all other traces out from under the die area
- When laser cutting, should also cut hole for HV contact. AGnd ring should be further away from hole, and some better way to get HV bias contact in from outside should be found (we used long wirebond over kapton tape).
- Continue to have occasional problems bonding to AMS chips. Typically one pad where on second bonding attempt, Al flakes off and connection must be hand epoxied.
- Critical to eliminate all small voids in film adhesive between Flex and module to avoid impossible wire-bonds. Also concerns with strength of Flex bond...
- Resistance of traces is rather high (U-shaped bus has about 10Ω resistance for thin signal line). Also, add extra vias to power bussing
- Consider realistic decoupling needs and possibly enhance this on present design
- Incorporate VCal on Flex layout
- Implement HitBus support and other mods on Flex Support board

Some comments on decoupling parts:

- Can find 0.047 μF 16V X7R in 0402 package, or 0.1 μF Y5V
- Can find 0.22 μF 10V X7R in 0603 package, or 1.0 μF 10V in Y5V
- X7R is preferred for noise, temperature coefficient and voltage coefficient reasons
- Can find 1 μF 6.3V Tantalum in 0603 package, or 0.68 μF 10V
- Can find 6.8 μF 6.3V Tantalum in 0805 package, or 4.7 μF 10 V

Suggest:

- We need to do a real SPICE simulation of our power distribution network, using real RLC models for the decoupling elements and power busses, and examining how transients are damped.
- We need to study in more detail the power-supply rejection of our front-ends as well, to match our decoupling to the FE needs.
- We may need to improve this aspect of our FE design before the next submissions !